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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,676	12/15/2003	Mitsuhiko Ogihara	MAE 304	6298
23995	7590	03/13/2006	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005				SMOOT, STEPHEN W
ART UNIT		PAPER NUMBER		
				2813

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/734,676	OGIHARA ET AL.
	Examiner	Art Unit
	Stephen W. Smoot	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 November 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 3,4,10,12-15,18,19 and 26-39 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 19 is/are allowed.
- 6) Claim(s) 3,4,10,12,15,18,26-32 and 39 is/are rejected.
- 7) Claim(s) 13,14 and 33-38 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 15 December 2003 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 16 November 2005.

Allowable Subject Matter

1. The indicated allowability of claims 3-4, 10, 12, 15, 18 is withdrawn in view of the newly discovered reference to Gonzalez et al. (US 6,429,070 B1). Rejections based on the newly cited reference follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3-4, 10, 12, 15, 18, 26-30, 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Gonzalez et al. (US 6,429,070 B1).

Referring to Fig. 12 and column 3, line 35 to column 8, line 22, a structure corresponding to DRAM cells that includes a monocrystalline silicon substrate (12) with overlying integrated DRAM capacitors (50, 52) thereon, a silicon containing layer (70) (e.g. undoped amorphous silicon) disposed on the substrate (12), a second monocrystalline silicon base (72) bonded to the silicon-containing layer (70), and transistor devices (100, 102) formed over and within the semiconductor base (72). Note that semiconductor base is very broadly defined by Gonzalez et al. and can include a semiconductor material layer (see column 3, lines 40-48) or, in other words, can be a semiconductor thin film. Also note that the base material can be an alternative semiconductor material like germanium (see column 6, lines 45-50). These are all of the limitations set forth in claims 18, 26-29, 39 of the applicant's invention.

Further regarding claims 3-4, an insulating layer (40) that can be silicon dioxide is disposed between the substrate (12) and the silicon-containing layer (70) (see column 4, lines 49-50).

Further regarding claim 10, trenches can be formed in portions of the base (72) and refilled with conductively doped semiconductive material to form doped regions (136, 138, 140) as described in column 7, lines 43-50.

Further regarding claims 12, 15, heavily doped source/drain region (136a, 140a) can extend from the top of the base (72) through the silicon-containing layer (70) to

directly contact storage node masses (46, 48) as described in column 8, lines 3-22)
(also see Fig. 19).

Further regarding claim 30, an insulating layer (14) is formed over the monocrystalline silicon substrate (12).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez et al. (US 6,429,070 B1) as applied to claim 26 above, and further in view of Jackson et al. (US 5,081,513).

As shown above, Gonzalez et al. anticipate claim 26 of the applicant's invention. Also, Gonzalez et al. teach that the silicon-containing layer can be amorphous silicon (see column 6, lines 18-23) and suggest that monocrystalline germanium can be used as an alternative material to monocrystalline silicon (see column 6, lines 45-50), which anticipate further limitations to claim 26 as set forth in claim 31 of the applicant's invention. However, although Gonzalez et al. do teach alternative semiconductor materials, they do not expressly teach or suggest a compound semiconductor thin film,

which is a further limitation to claim 26 as set forth in both claim 31 and claim 32.

Jackson et al. suggest that gallium arsenide can be used as a semiconductor thin film for thin film transistors (see Fig. 5 and column 4, lines 9-38).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Gonzalez et al. and Jackson et al. in order to substitute a gallium arsenide thin film, as suggested by Jackson et al., for the silicon base of Gonzalez et al. Jackson et al. recognize that gallium arsenide is an alternative semiconductor material that can be used as a charge transport layer in thin film transistors (see column 4, lines 28-32).

Allowable Subject Matter

6. Claim 19 is allowed.

7. Claims 13-14, 33-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

- Claims 13-14 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a semiconductor

structure that includes an adhesion layer mainly consisting of semiconductor material disposed on a substrate and a semiconductor thin film bonded on the adhesion layer, further comprising an interconnecting layer for electrically connecting a semiconductor device that corresponds to the semiconductor thin film to an integrated circuit that corresponds to the substrate, wherein an interdielectric layer electrically isolates the interconnecting layer from the semiconductor thin film;

- Claim 19 is allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, a semiconductor structure that includes an adhesion layer mainly consisting of semiconductor material disposed on a substrate and a semiconductor thin film bonded on the adhesion layer, wherein a plurality of semiconductor thin films are arranged on the adhesion layer at regular intervals;
- Claim 33 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a semiconductor structure that includes an adhesion layer mainly consisting of semiconductor material disposed on a substrate and a semiconductor thin film bonded on the adhesion layer, wherein a main constituent of the adhesion layer is different from a main constituent of the semiconductor thin film, wherein the semiconductor material has an affinity to both the semiconductor thin film and the substrate and wherein the semiconductor thin film includes at least one semiconductor device

that is any of a light emitting element, a light sensing element, a Hall element, or a piezoelectric element; and

- Claims 34-38 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, an optical print head with a semiconductor structure that includes an adhesion layer mainly consisting of semiconductor material disposed on a substrate and a semiconductor thin film bonded on the adhesion layer, wherein a main constituent of the adhesion layer is different from a main constituent of the semiconductor thin film, and wherein the semiconductor material has an affinity to both the semiconductor thin film and the substrate.

Response to Arguments

9. Applicant's arguments with respect to claims 26-32, 39 have been considered but are moot in view of the new grounds of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws


STEPHEN W. SMOOT
PRIMARY EXAMINER